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# A LOW COMPLEXITY SLM SCHEME FOR PAPR REDUCTION OF OFDM SIGNALS

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**ABSTRACT:** The selected mapping (SLM) is an effective technique for peak-to-average power reduction (PAPR) of orthogonal frequency division multiplexing (OFDM) signals. SLM has high computational complexity due to the computation of multiple IFFTs. In this paper, low complexity SLM is proposed based on a novel simplified IDFT algorithm developed such that it does not involve any complex arithmetic. The proposed SLM, with $U$ candidate signals, achieves a computational complexity reduction ratio of $\left(1-\frac{1}{U}\right)\%$ with respect to traditional SLM. This reduction is at the expense of using limited memory and negligible degradation in PAPR reduction performance. The computational core of the proposed SLM is implemented on the Spartan 3E XC3S500E FPGA platform to highlight its hardware implementation issues and to verify its effectiveness.
**KEYWORDS:** Selected Mapping (SLM), Peak-to-Average Power Ratio (PAPR), Orthogonal Frequency Division Multiplexing (OFDM), Simplified IDFT, Field Programmable Gates Array (FPGA)

## 1. INTRODUCTION

The rising popularity of Orthogonal Frequency Division Multiplexing (OFDM) in wireless and wireline applications is mainly due to its immunity to multipath fading and impulse noise, and its efficient hardware implementation using FFT techniques [1]. OFDM is adopted in many high speed applications such as WiFi, WiMAX, DVB, DSL, etc [1-3].

However, OFDM suffers from the drawback that the transmitted signal can exhibit a large peak-to-average power ratio (PAPR). This requires that the transmit power amplifier to operate in its linear region with a large input back-off where the power conversion becomes inefficient. In many low cost applications the problem of high PAPR may outweigh all the potential benefits of OFDM [1]. Several techniques have been developed to reduce PAPR [4]. The Selected Mapping (SLM) is considered in this paper. It is an effective distortionless technique capable of achieving significant PAPR reduction with only a small amount of redundancy [5].

In traditional SLM (T-SLM), the original OFDM symbol $\boldsymbol{S}=\{S_k: 0 \le k \le N-1\}$ is multiplied by a set of $U$ independent phase steering vectors, $\boldsymbol{P}^u$, to produce the $U$ frequency domain alternative OFDM symbols [6]

$$\boldsymbol{S}^u=\boldsymbol{S}\odot\boldsymbol{P}^u \qquad 1 \le u \le U \tag{1}$$

where $\odot$ is the element wise multiplication operator and $\boldsymbol{P}^u=[p_0^u, p_1^u, \dots, p_{N-1}^u]$ with $p_k^u=\exp(j\emptyset_k^u)$ and $\emptyset_k^u$ are randomly chosen from $[0,2\pi)$, so that typically $p_k^u \in\{\pm1, \pm j\}$ [7]. For better approximating the actual peak of the analog transmitted signal, the symbols $\boldsymbol{S}^u$ are oversampled $L$ times [3]. An oversampled alternative symbol, $\boldsymbol{X}^u$, is obtained by inserting

$N(L-1)$ zeros into the middle of the symbol $\boldsymbol{S}^u$. Then, the $U$ time domain candidate signals, $\boldsymbol{x}^u$, are the IFFT of $\boldsymbol{X}^u$, given by [2]

$$x_n^u = \sum_{k=0}^{NL-1} X_k^u \, e^{j2\pi kn/NL} \qquad 0 \le n \le NL-1 \tag{2}$$

The candidate signal $\boldsymbol{x}^u$ of the minimum PAPR is selected and transmitted together with its index $u = arg\{\boldsymbol{x}^u\}$ as side information, where the PAPR is defined by [2]

$$PAPR = 10\, log_{10} \frac{max_{0\le n\le NL-1}(|x_n^u|^2)}{E[|x_n^u|^2]} \tag{3}$$

The computational complexity of the T-SLM using *U NL*-point IFFT operations, is too high to be acceptable in practical applications [8]. A number of schemes have been presented in the literature to reduce the computational complexity of the SLM. In [2],[9], some of the IFFT blocks of the SLM are replaced by conversion matrices constructed from the phase steering vectors. This approach achieves comparable PAPR reduction with respect to T-SLM with much lower complexity but degraded Bit Error Rate (BER) performance. Another approach proposes the product of the phase vectors by intermediate signals within the IFFT, as in [8], or by a subset of the intermediate signals as in [4]. The PAPR reduction in this approach degrades as the number of stages remaining after phase vector multiplication decreases. Moreover, low complexity SLMs those use time domain symbol processing to generate multiple candidate signals are presented in [10-14]. In spite of lower complexity, these schemes show poorer PAPR reduction performance with respect to T-SLM.

In this paper, a low complexity SLM scheme is proposed. It employs a Simplified IDFT (SIDFT) algorithm developed in this paper for PSK and QAM modulated OFDM symbols. The SIDFT is used to transform the alternative OFDM signals to approximated time domain candidate signals. Then, the signal of minimum PAPR is determined and the corresponding alternative OFDM symbol is transformed using an ordinary *NL*-point IFFT to get the transmitted signal. The SIDFT algorithm does not use complex arithmetic operations (neither multiplications nor additions), instead, it reads data from prestored seed vectors in a proper way and uses them to increment or decrement a set of up/down counters whose final contents represent the approximated time domain signal samples. Therefore, the computational complexity of the proposed SLM (P-SLM) is much less than that of an equivalent T-SLM.

The rest of the paper is organized as follows: The SIDFT is developed in Section II. The P-SLM is presented in Section III. In Section IV, the computational complexity of the P-SLM is compared with T-SLM and other low complexity SLM schemes. In Section V the PAPR reduction performance of the P-SLM is evaluated. Finally, concluding remarks are given in Section VI.

## 2. SIMPLIFIED IDFT

The SIDFT is a low complexity IDFT developed in this paper to be used in SLM technique employing PSK or QAM modulated OFDM symbols. The SIDFT algorithm depends on the fact that the complex multiplication and addition operations of an ordinary IDFT are separable. That is, to transform an alternative OFDM symbol $\boldsymbol{X}^u$, then firstly each of its subsymbols, $X_k^u$ for $0 \le k \le NL-1$, is multiplied by the $(k+1)^{th}$ IDFT basis row vector to produce the $NL \times NL$ matrix $\boldsymbol{A}$ given by

$$\boldsymbol{A} = \begin{bmatrix} X_0^u & \cdots & X_0^u & \cdots & X_0^u \\ X_1^u & \cdots & X_1^u e^{\frac{j2\pi k}{NL}} & \cdots & X_1^u e^{\frac{j2\pi(NL-1)}{NL}} \\ X_2^u & \cdots & X_2^u e^{\frac{j4\pi k}{NL}} & \cdots & X_2^u e^{\frac{j4\pi(NL-1)}{NL}} \\ & & \vdots & & \\ X_{NL-1}^u & \cdots & X_{NL-1}^u e^{\frac{j2\pi(NL-1)k}{NL}} & \cdots & X_{NL-1}^u e^{\frac{j2\pi(NL-1)^2}{NL}} \end{bmatrix} \quad (4)$$

Secondly, the $(i+1)^{th}$ sample of the time domain signal, $x_i^u$ for $0 \le i \le NL-1$, is the sum of the elements of the $(i+1)^{th}$ column of $\boldsymbol{A}$.

$$x_i^u = \sum_{\substack{k=0 \\ k \neq \frac{N}{2},\dots,NL-\frac{N}{2}-1}}^{NL-1} A_{k,i} \quad 0 \le i \le NL-1 \quad (5)$$

Having the middle $N(L-1)$ elements of $\boldsymbol{X}^u$ are zeros, then the $N(L-1)$ rows of $\boldsymbol{A}$ are also all zeros, therefore, the range of $k$ values ( $\frac{N}{2} \le k \le NL - \frac{N}{2} - 1$) is excluded in equation (5).

However, significant simplifications to the multiplications and additions are possible while keeping the algorithm sufficient to be used in a SLM. That is, for a given $M$-PSK signal constellation, with possible signal values $\{c_n: 0 \le n \le M-1\}$, $\boldsymbol{A}$ can be constructed from a set of $M$ prestored seed vectors. These vectors are generated by multiplying the IDFT basis vector $e^{j2\pi i/NL}$ for $0 \le i \le NL-1$, by each possible signal value. Resulting in an $NL$-element seed vector, $\boldsymbol{D}_n$ for each possible OFDM subsymbol value.

$$\boldsymbol{D}_n = \left\{ D_{n,i} = c_n e^{\frac{j2\pi i}{NL}}: 0 \le i \le NL-1 \right\} \quad (6)$$

for $0 \le n \le M-1$.

For a given OFDM symbol $\boldsymbol{X}^u$, the $(k+1)^{th}$ row of $\boldsymbol{A}$, for $(0 \le k \le NL-1)$ and $k \neq (\frac{N}{2},\dots,NL-\frac{N}{2}-1)$, denoted by $\boldsymbol{A}_k$, is constructed for the subsymbol $X_k^u$ by selecting the seed vector $\boldsymbol{D}_n$ such that $n = arg\{X_k^u = c_n\}$ and then cyclically sampling this seed vector, thus

$$\boldsymbol{A}_k = \left\{ D_{n,(ik)modNL}: 0 \le i \le NL-1 \right\} \quad (7)$$

The generation of $\boldsymbol{A}$ by this technique neglects all of the complex multiplications during the dynamic operation mode of the SIDFT algorithm. However, the $(M \times NL)$ complex multiplications needed to generate the $M$ seed vectors are implemented once before the dynamic operation mode of the system.

Next, the elements of the $(i+1)^{th}$, $0 \le i \le NL-1$, column of $\boldsymbol{A}$ are supposed to be summed to determine the time domain sample $x_i^u$. Basically, this costs $NL(N-1)$ complex additions to produce the signal $\boldsymbol{x}^u$. Instead of that, it is proposed in this paper to quantize the real and imaginary components of $\boldsymbol{A}$ to the nearest integer, and use them to increment or decrement two up/down simple binary counters per signal sample such that their final contents are the approximated signal samples, $\hat{x}_i^u$.

Let $r_{k,i}$ and $q_{k,i}$ be the real and imaginary components of $A_{k,i}$, and their quantized versions are $\bar{r}_{k,i}$ and $\bar{q}_{k,i}$, respectively. Then the values of $\bar{r}_{k,i}$ elements belonging to the $(i+1)^{th}$ column of $\boldsymbol{A}$ are used to increment ($\bar{r}_{k,i} > 0$), decrement ($\bar{r}_{k,i} < 0$) or unchanged ($\bar{r}_{k,i} = 0$) an initially reset binary up/down counter, whose final value is the real part of the approximated sample $\hat{x}_i^u$. The imaginary component of $\hat{x}_i^u$ is obtained from $\bar{q}_{k,i}$ in a similar manner without performing any complex addition operation.

A total of $2NL$ simple up/down counters are required to accommodate the $NL$ samples of an approximated time domain signal $\widehat{\boldsymbol{x}}^{u}$. For more simplicity, the quantization can be performed initially on the elements of the seed vectors such that the elements of $\boldsymbol{A}$ are already quantized. To avoid the need for a memory to store the matrix $\boldsymbol{A}$, then its elements, $A_{k,i}$, are generated and used in an in-place manner. That is, once an $A_{k,i}$ is generated by equation (7), it is used to update the corresponding result counter and then discarded to process the next element of $\boldsymbol{A}$, and so on.

Being an essential requirement in the SIDFT that $\bar{r}_{k,i}$ are integers, it results in a course quantization to $r_{k,i}$ when the difference between their values, denoted by $\Delta r$, is less than 0.5. That is, all $r_{k,i}$ values within the interval $[\bar{r}-0.5, \bar{r}+0.5)$ will be quantized to $\bar{r}_{k,i}$. The problem becomes worse for large signal constellations when $\Delta r$ becomes smaller. This leads finally to low accuracy samples of the approximated time domain signal. To enhance this accuracy, the dynamic range of $r_{k,i}$ values is increased before being quantized. The integer part of $r_{k,i}$ is extended by including digits from the fractional part. This is achieved by shifting the decimal point to the right such that a predetermined number of integer digits, $b$, of $\bar{r}_{k,i}$ is obtained. Then, the maximum $\bar{r}_{k,i}$, determines the required number of bits to store $\bar{r}_{k,i}$ to be $\lceil log_2(10^b-1)\rceil$ and the number of bits of the real component result counter to be $\lceil log_2(N(10^b-1))\rceil$, where $\lceil . \rceil$ returns the smallest greater integer. The same analysis is applicable to the quantization of the imaginary components of seed vector elements $q_{k,i}$.

As a result, the SIDFT does not involve complex multiplications nor additions. It uses a limited memory of $(M \times 2NL)$ locations to store $M$ seed vectors each of $NL$ elements, by assuming that a location stores a real or imaginary component of an element. For example, for QPSK modulated OFDM symbols with $N = 256$ and $L = 4$, then, 8192 memory locations are required to store the seed vectors. However, due to quantization, the sample values, $\hat{x}_i^u$, and hence the PAPR of the time domain signals produced by the SIDFT are not identical to those produced by ordinary IDFT, $x_i^u$. But, from a SLM system point of view, SIDFT is applicable as long as the relative PAPR values among the $U$ approximated signals, $\widehat{\boldsymbol{x}}^{u}$ are similar to those of exact candidate signals, $\boldsymbol{x}^{u}$. The PAPR reduction performance of the P-SLM based on the SIDFT is discussed in section V.

## 3. PROPOSED SLM

The block diagram of the P-SLM is shown in Fig.1. For an OFDM symbol, $\boldsymbol{S}$, the $U$ alternative symbols are generated. Each alternative symbol, $\boldsymbol{S}^{u}$ is fed to an SIDFT block such that

$$X_k^u = \begin{cases} S_k^u & 0 \le k \le \frac{N}{2}-1 \\ S_{N-NL+k}^u & NL-\frac{N}{2} \le k \le NL-1 \end{cases} \quad (8)$$

and transformed to its corresponding approximated time domain signal, $\widehat{\boldsymbol{x}}^{u}$. Then, the index, $\acute{u}$, of the signal with the minimum PAPR is determined and prepared to be sent to the receiver as side information. The index $\acute{u}$ is also used to pass the corresponding alternative symbol, $\boldsymbol{S}^{\acute{u}}$, to the 'Oversampling and $NL$-IFFT' block. The latter computes the ordinary IFFT of the $L$-times oversampled version of $\boldsymbol{S}^{\acute{u}}$, to produce the transmit signal, $\boldsymbol{x}^{\acute{u}}$. The same T-SLM receiver can be used with the P-SLM scheme.

However, initially, the memory is loaded by the $M$ quantized seed vectors. They are generated according to the used subsymbol constellation and the number of subcarriers, $N$, as described in section II. Due to their simplicity, the SIDFT blocks can be implemented to operate in parallel. Theoretically, the total memory size required is $(M \times 2NL)$ locations, but practically some additional temporary storage may be needed to manage the concurrent requests to access the seed vector memory by the $U$ parallel SIDFT blocks.

The P-SLM employs only one IFFT operation, therefore, it involves much less complex computations, especially for large $U$, as compared with T-SLM and other low complexity SLMs presented yet in the literature. This significant reduction in computational complexity is achieved without sacrificing the BER performance since the magnitudes of the modulated subsymbols of the transmit signal are not distorted.

## 4. COMPUTATIONAL COMPLEXITY

The computational complexity of the P-SLM is compared with that of the T-SLM in terms of the number of complex multiplications, $C_{mul}$, and complex additions, $C_{add}$ during the dynamic mode of operation of the SLM. A T-SLM using $U$ $NL$-point IFFTs requires a $C_{mul}$ of $\frac{1}{2}UNL\, log_2 NL$ and a $C_{add}$ of $UNL\, log_2 NL$. The P-SLM uses only one $NL$-point IFFT with the other system modules do not include any complex arithmetic. Then, it requires a $C_{mul}$ of $\frac{1}{2}NL\, log_2 NL$ and a $C_{add}$ of $NL\, log_2 NL$. The computational complexity reduction ratio (CCRR), for both $C_{mul}$ and $C_{add}$, of the P-SLM with respect to T-SLM is $(1-\frac{1}{U})\%$, where the CCRR is defined by [3]

$$CCRR = \left(1 - \frac{complexity\ of\ P-SLM}{complexity\ of\ T-SLM}\right)\% \quad (9)$$

The CCRR is independent of $N$, $M$ and signal modulation. It reversely proportional with $U$, so that for the typical values of $U = 8, 16,$ and $32$, the CCRR is 87.5%, 93.75%, and 96.9%, respectively. Moreover, Table (1) presents a comparison between the P-SLM and a set of the main low complexity SLM schemes in the literature. The comparison is performed in terms of the CCRR of $C_{mul}$ and $C_{add}$ for $U = 16, L = 4$ and $N = 256, 512,$ and $1024$. Table (1) shows that the P-SLM is capable of achieving significant reductions in both $C_{mul}$ and $C_{add}$ greater than the presented low complexity SLM schemes. Therefore, the P-SLM is the best in this respect.

## 5. COMPUTER SIMULATION

The P-SLM and T-SLM are simulated using Matlab for 64-PSK modulated OFDM symbols with $p_k^u \in \{\pm 1, \pm j\}$, $U = 16$, $L = 4$, and $N = 256$ and $512$, to evaluate and compare their PAPR reduction performance. The seed vectors are generated with the real and imaginary components of their elements are amplified and then quantized such that $b = 2$. Meaning that, each single component occupies a 7-bit memory location. The total number of memory locations needed to store the 64 seed vectors and the largest size of each result counter measured in bits, are given in Table (2) for $N = 256$ and 512. These memory requirements are easily achievable on most available programmable hardware ICs, making the implementation of the SIDFT based SLM reasonable. The flowchart of the simulation program is shown in Fig. 2.

The complementary cumulative density function (CCDF) for the PAPR of the transmit signals is evaluated and plotted in Fig. 3 for $10^5$ independent randomly generated OFDM symbols. These plots show that the quantization used by the SIDFT just slightly affects the P-SLM performance. However, this slight difference in PAPR reduction is due to the approximated candidate signals whose PAPR values may not be accurate enough to identify the OFDM symbol $\boldsymbol{S}^u$ of the minimum PAPR. So, the P-SLM may suggest a symbol of some close but higher PAPR to be transformed and then transmitted. The results of Fig. 3 show that the effect of this inaccuracy is negligible on the PAPR reduction performance of the P-SLM.

## 6. FPGA IMPLEMENTATION OF P-SLM

In order to prove the simplicity and low complexity of the P-SLM in practice for real time applications, the computational core SIDFT algorithm of P-SLM scheme is realized in hardware. The proposed architecture of the SIDFT is illustrated in Fig. 4. It involves three separated memory modules, namely the signal ROM, seed vectors ROM and matrix RAM. The PSK modulated symbols are stored in the signal ROM such that each symbol is represented by 2 bits (logic 0 for positive real or imaginary term and logic 1 for negative). The seed vectors ROM is used to store the offline computed seed vectors, $\boldsymbol{D}_n$, given by equation (6) that are used to construct the elements of the matrix $\boldsymbol{A}$ given by equation (4) to be then written on the matrix RAM.

In this paper, QPSK modulated OFDM symbols with $N$=8 are implemented. Then, the required sizes for the three memory modules become (2 bits × 8) for the signal ROM, (4bits × 32) for seed vectors ROM and (4 bits × 64) for matrix RAM. The computed four seed vectors for the QPSK symbols $\{\pm 1, \pm j\}$ are given in Table (3). By quantizing these seed vectors into the nearest integer, it results in values belonging to $\{0, \pm 1, \pm j\}$. Then, their binary representation is modified to signed binary form by allocating 2 bits for the real part and 2 bits for the imaginary part. The seed vectors become as given in Table (4).

The quantized binary seed vectors are stored in the 32 locations of the seed vector ROM by arranging them into four segments. Segment 1 includes the first eight locations to store the eight elements of the first seed vector. Segment 2 includes the second eight locations to store the eight elements of the second seed vector and so on. The symbol itself that is read from signal ROM is used as the two most significant address lines to select the appropriate segment within the seed vector ROM that includes the corresponding seed vector row. The other three address lines are generated by the system controller to select the appropriate seed vector elements according to the step value (position within the OFDM block) of the current input symbol index. Then, these seed vector elements are written to the matrix RAM to be used to increment or decrement the up/down result counter later. The final result is represented by 10 bits (5 bits for each real and imaginary part). The system controller generates all addresses and control signals for the three memory modules and the counter during system operation.

## 7. FPGA IMPLEMENTATION RESULTS

In this paper, the Spartan-3E XC3S500E FPGA platform is used with the aid of the Xilinx ISE 9.2i design package for simulation and programming using the VHDL language. Fig. 5 shows a part from the test bench waveform simulation. Its shows how the signal ROM outputs a specific symbol and waits 8 clock cycles for reading the corresponding 8 seed vector row elements to be saved in the matrix RAM and the status of control signals during operation. Table (5) lists the device utilization summary given by the ISE utilization summary report. The implementation report shows that the design can operate with a maximum frequency up to 123.709 MHz.

## 8. CONCLUSION

A simplified algorithm for the IDFT, called the SIDFT, is developed in this paper. It does not involve any complex arithmetic, instead, it reads previously stored data and uses them to increment or decrement the result registers. The time domain signals produced by the SIDFT are not identical to those of ordinary IDFT, but they have PAPR values sufficient to identify an OFDM symbol of an acceptably small PAPR among the $U$ alternative symbols in a SLM. A SLM scheme based on the SIDFT is proposed. The P-SLM uses only one ordinary IFFT, therefore it achieves a CCRR of 93.75% for both $C_{mul}$ and $C_{add}$ with respect to T-SLM when $U = 16$. In this respect, the P-SLM is simpler than the main low complexity SLMs presented in the literature. However, this great reduction in computational complexity is at the expense of using a limited storage memory and a negligible degradation in PAPR reduction performance. The FPGA implementation of the computational core of the P-SLM has verified its simplicity and effectiveness. Therefore, it seems that the P-SLM is a perfect candidate to replace T-SLM in practical applications.

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**Table (1):** CCRR (%) of $C_{mul}$ and $C_{add}$ of the P-SLM and other low complexity SLM schemes with respect to T-SLM for $U = 16, L = 4$ and $N = 256,\ 512,$ and $1024$.

| $N$ | CCRR of | SLM Scheme | | | | | |
|---|---|---|---|---|---|---|---|
| | | P-SLM | [8] | [9] Scheme I | [9] Scheme II | [7] | [14] |
| 256 | $C_{mul}$ | 93.75 | 92.031 | 93.75 | 87.5 | 60 | 62.5 |
| | $C_{add}$ | 93.75 | 71.25 | 65.625 | 61.25 | 67.5 | 50.006 |
| 512 | $C_{mul}$ | 93.75 | 96.378 | 93.75 | 87.5 | 61.364 | 62.5 |
| | $C_{add}$ | 93.75 | 73.864 | 68.182 | 63.636 | 68.182 | 51.14 |
| 1024 | $C_{mul}$ | 93.75 | 98.34 | 93.75 | 87.5 | 62.5 | 62.5 |
| | $C_{add}$ | 93.75 | 76.042 | 70.313 | 65.625 | 68.75 | 52.085 |

**Table (2):** Memory requirements of the simulated P-SLM

| N | number of memory locations to store the 64 seed vectors | Single result counter size in bits |
|---|---|---|
| 256 | 131072 | 15 |
| 512 | 262144 | 16 |

**Table (3):** Seed Vectors

| symbol | corresponding seed vector | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 1+j | 1+j | 1.4j | -1+j | -1.4 | -1-j | -j1.4 | 1-j | 1.4 |
| 1-j | 1-j | 1.4 | 1+j | j1.4 | -1+j | -1.4 | -1-j | -1.4j |
| -1+j | -1+j | -1.4 | -1-j | -j1.4 | 1-j | 1.4 | 1+j | 1.4j |
| -1-j | -1-j | -1.4j | 1-j | 1.4 | 1+j | 1.4j | -1+j | -1.4 |

**Table (4):** Quantized binary represented seed vectors

| symbol | corresponding seed vector | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 00 | 0101 | 0001 | 1101 | 1100 | 1111 | 0011 | 0111 | 0100 |
| 01 | 0111 | 0100 | 0101 | 0001 | 1101 | 1100 | 1111 | 0011 |
| 10 | 1101 | 1100 | 1111 | 0011 | 0111 | 0100 | 0101 | 0001 |
| 11 | 1111 | 0011 | 0111 | 0100 | 0101 | 0001 | 1101 | 1100 |

**Table (5):** Device utilization summary

| Logic Utilization | Used | Available | Utilization |
|---|---|---|---|
| Number of Slices | 40 | 4656 | 0% |
| Number of Slice Flip Flops | 48 | 9312 | 0% |
| Number of 4 input LUTs | 80 | 9312 | 0% |
| Number of bonded IOBs | 14 | 232 | 6% |
| Number of BRAMs | 3 | 20 | 15% |
| Number of GCLKs | 1 | 24 | 4% |

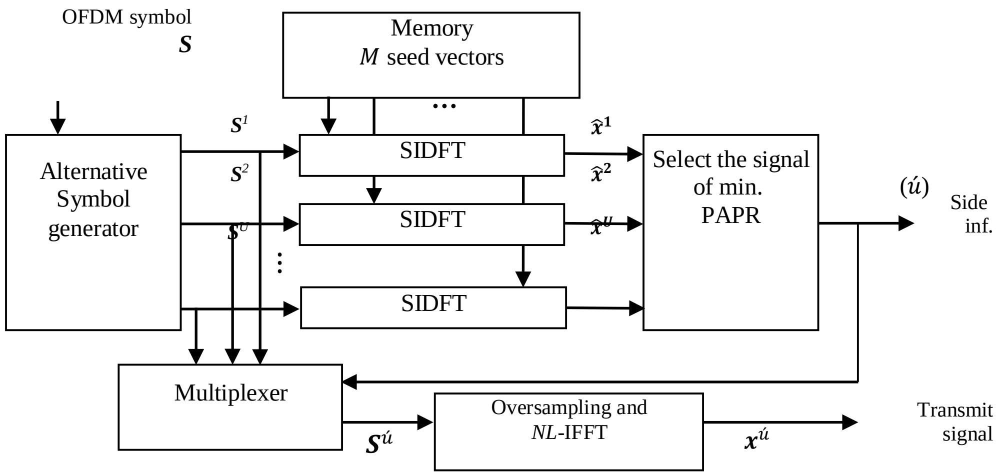


**Fig.1:** Proposed SLM scheme

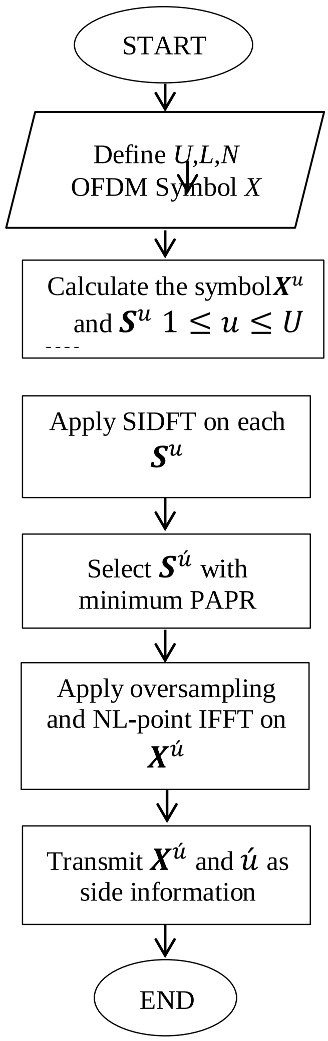


**Fig. 2:** Flowchart of the simulation program

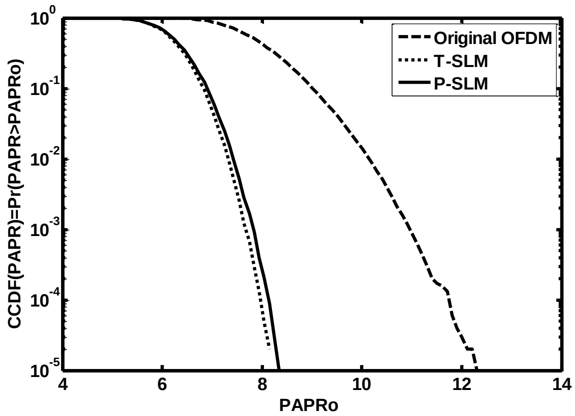


**Fig. 3(a):** PAPR reduction performance of P-SLM and T-SLM for $U$=16, $L$=4, and 64-PSK modulated OFDM signal with $N$=256

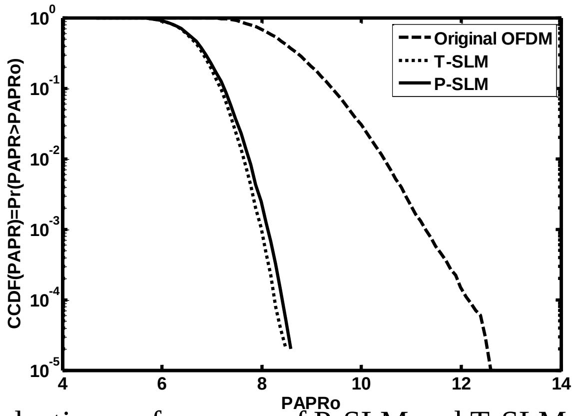


**Fig. 3(b):** PAPR reduction performance of P-SLM and T-SLM for $U$=16, $L$=4, and 64-PSK modulated OFDM signal with $N$=512

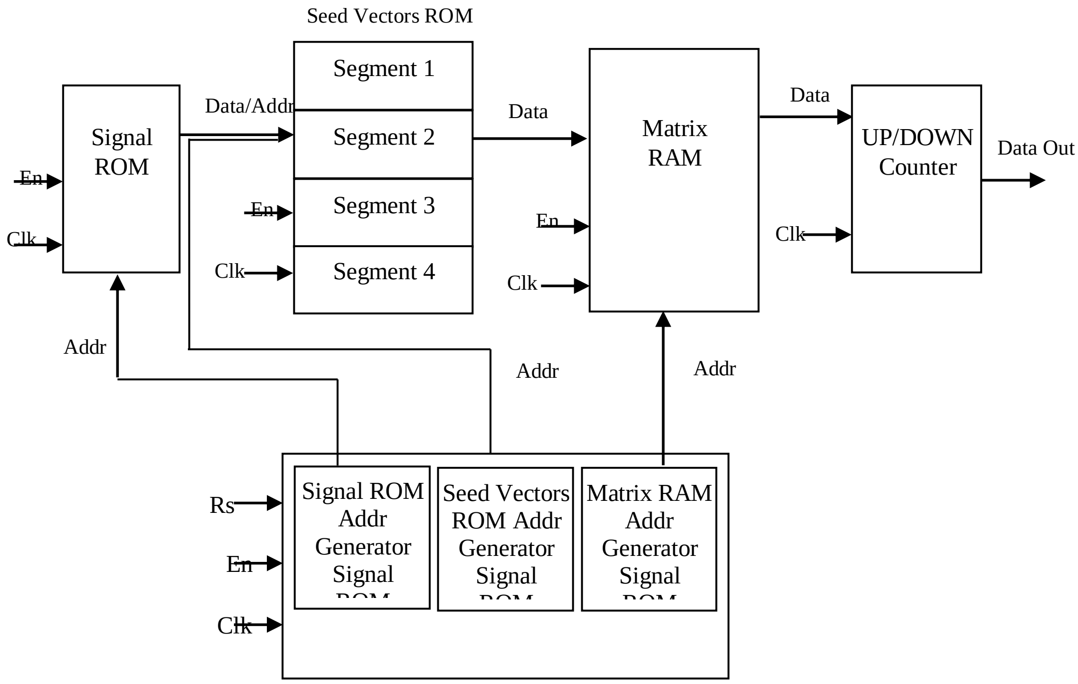


**Fig. 4:** General diagram of the implemented system

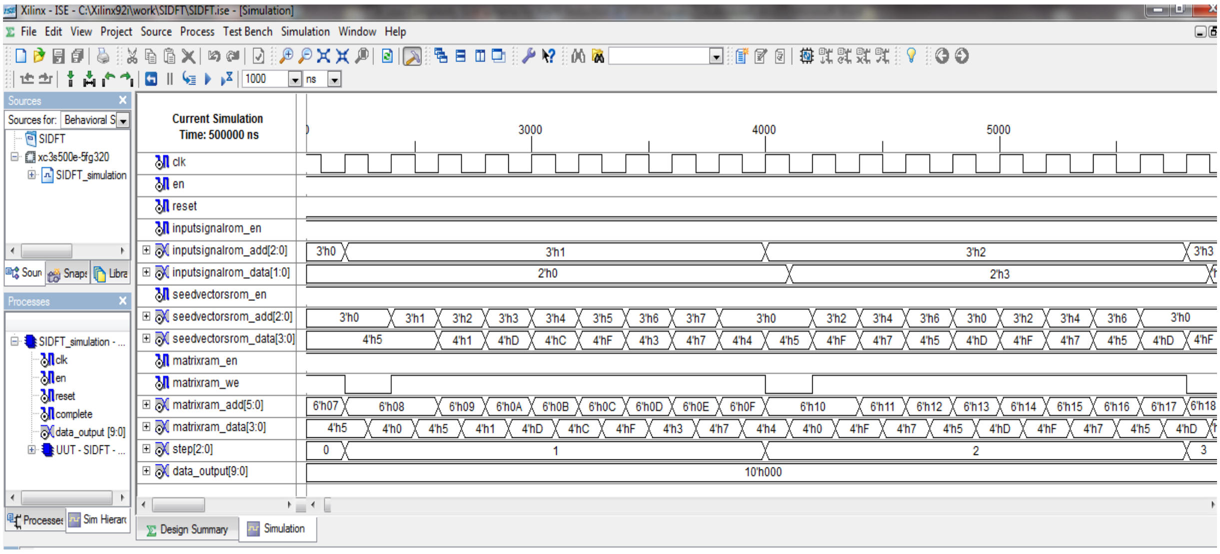


**Fig. 5:** Simulation test bench waveforms

# تقنية SLM منخفضة التعقيد لتقليل نسبة الذروة الى المعدل لقدرة الاشارات المرسلة في انظمة OFDM

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**الخلاصة:**

تعتبر تقنية التنظيم المختار (SLM) من الطرق الفعالة في تقليل نسبة الذروة الى المعدل (PAPR) لقدرة الاشارات المرسلة في انظمة التضمين ذات القنوات المتعددة المتعامدة (OFDM). و لكن درجة تعقيد الحسابات لتقنية (SLM) عالية نسبيا بسبب تظمنها لعملية حساب محول فورير العكسي لعدة مرات لتوليد عدد من الاشارات المرشحة للارسال. في هذا البحث، تم اقتراح طريقة لتخفيض تعقيد تقنية (SLM) بالاعتماد على اقتراح خوارزمية مبسطة لمحول فورير العكسي لا تتضمن اية حسابات مركبة. ان تقنية (SLM) المقترحة التي تولد $U$ من الاشارات المرشحة للارسال، تحقق نسبة تخفيض في درجة تعقيد الحسابات تقدر بـ $\%\left(1-\frac{1}{U}\right)$ بالمقارنة مع التقنية التقليدية. هذه النسبة لا تعتمد على عدد النواقل و لكنها تكون على حساب الحاجة لاستخدام ذاكرة بمساحة خزن محدودة و انخفاض طفيف في اداء تخفيض (PAPR). تم تنفيذ التقنية المقترحة باستخدام مصفوفة البوابات القابلة للبرمجة FPGA Spartan 3E XC3S500E لتسليط الضوء على تفاصيل التنفيذ العملي لها و للتحقق من فعاليتها.

**الكلمات المفتاحية:** تقنية التنظيم المختار (SLM)، نسبة الذروة الى المعدل للقدرة (PAPR)، انظمة التضمين ذات القنوات المتعددة المتعامدة (OFDM)، محول فورير العكسي المبسط، مصفوفة البوابات القابلة للبرمجة (FPGA)